

AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 2, line 14, with the following rewritten paragraph:

- 1 As computer systems started to utilize more graphic images and video
- 2 conferencing became more desirable, the communication of video data has
- 3 become important over both LANs and WANs. While separate means for
- 4 communication of video between end users could have been developed, it is
- 5 desirable to simultaneously communicate ~~communication~~ video data, audio data,
- 6 and digital data across a LAN and a WAN.

Please replace the paragraph beginning at page 5, line 15, with the following rewritten paragraph:

- 1 ATM networks communicate using cell switching which is a form of
- 2 asynchronous ~~Asynchronous~~ time division multiplexing. The cells ~~cell~~ used in
- 3 ATM are of a fixed length as opposed to packet switching which uses variable
- 4 length data packets.

Please replace the paragraph beginning at page 12, line 18, with the following rewritten paragraph:

1 Referring now to Figure 2 there is illustrated a block diagram of an
2 exemplary ATM module 101 in accordance with an embodiment of the present
3 invention. The ATM module 101 includes a module interconnect in the form of a
4 shared bus type arrangement with which all internal modules interface. The
5 internal modules include the main processing module or ATM processor 120,
6 UTOPIA L-2 module 108, Cell DMA I/F 106, Cell buffer module 104, AAL2
7 module 102, AAL5 module 105, and RAM module 112 which includes state RAM
8 and data memory. The ATM processor is the master to all other modules on the
9 peripheral interconnect. When the ATM module 101 is connected as a stand-
10 alone chip, a chip/peripheral interconnect module 140 can be included to couple
11 to a host processor system. Further, an interface module or HPI/XBUS/PCI
12 module 145 may be needed as an external interface with the cell DMA/ IF 106.

Please replace the paragraph beginning at page 18, line 6, with the following rewritten paragraph:

1 A novel aspect of the ATM module 101, which utilizes an ATM processor
2 120 to fetch/forward ATM cells from/to ports (e.g. UTOPIA Level 2 port 108, Cell
3 I/F port 106 etc.) and functions (e.g. AAL2 SAR 102, AAL5 SAR 105, Cell Buffer
4 104, etc.), allows for a function/feature rich ATM solution as well as enhanced
5 system performance by reducing the overhead on the host. As previously
6 mentioned, these functions can include ATM switching, Quality of Service (QoS),
7 and Operation ~~operation~~ and Maintenance (OAM) processing.

Please replace the paragraph beginning at page 29, line 5, with the following rewritten paragraph:

1 One disadvantage of this type of system is that data transmitted or
2 received must be written on the system bus twice (once between the host
3 processor and the DSP, and once between the host processor and the ATM
4 transport hardware), resulting in system performance degradation. Another
5 disadvantage is that very software intensive functions must be performed for
6 AAL2 transmit and receive, such as CRC and parity calculation. Hence, a
7 relatively powerful, host processor must be ~~be~~ used compared to if the AAL2
8 transmit and receive function had been done in dedicated hardware. Because of
9 at least the aforementioned disadvantages, this architecture also does not scale
10 very well to dense voice solutions.

Please replace the paragraph beginning at page 37, line 15, with the following rewritten paragraph:

1 More particularly, referring to Figure 5 there is illustrated a function block
2 diagram of an AAL2 ~~AAL~~ receiver 950 in accordance with an exemplary
3 embodiment of the present invention. The AAL2 receiver 950 can be
4 implemented in hardware in the ATM module 102. The AAL2 receiver 950 has
5 two sets of DMAs associated with the AAL2 RX DMA 515 which are directly
6 interfacing with the DSP 412A and DSP 412B, respectively, DSP(s) 160 and the
7 host 414 490 (i.e. processing element): Channels 1-4 and channels 5-8 of the
8 DSP DMA DMA(s) - write writes AAL2 voice packets to the DSP 412A and DSP
9 412B, respectively, DSP(s) 160 and the single channel 9 of the HOST DMA -
10 writes AAL2 signaling/management packets to the host 414 490.

Please replace the paragraph beginning at page 38, line 11, with the following rewritten paragraph:

1 The Reassembly Engine 520 checks the CPS packet header's HEC, and
2 determines if the CPS-packet(s) should be forwarded to one of the DSPs (A or
3 B) Rx FIFOs (540, 541) or the Rx Host FIFO 530 as follows. The AAL2 receive
4 engine allows the host 414 ~~190~~ to configure CPS-packets to be filtered to the
5 host 190 on CID or UUI information. Hence, the host 414 ~~190~~ can receive CPS-
6 signaling packets and peer-to-peer layer management packets. If a match was
7 made in the CID Filter 550, then the packet will be forwarded to the host 414 ~~190~~
8 and the UUI Filter 560 is not interrogated. If no match was made in the CID Filter
9 550, the UUI Filter 560 is searched. If a match is made in the UUI Filter 560 the
10 packet will either be forwarded to the Host DMA or discarded. (The UUI Filter
11 has a feature that allows the host to discard packets based on the UUI.)
12 Otherwise, if a CPS-packet's CID matches a CID in the AAL2 Rx LUT (LookUp
13 Table) 580, the packet is forwarded to one of the 9 channels (8 voice channels
14 and one host channel) in the Rx DMA RAM 590 according to the logical channel
15 number associated with that particular CID. The entries in the LUT 580 are
16 updated when the host software adds an AAL2 channel via the AAL2 Channel
17 Configuration Register.

Please replace the paragraph beginning at page 39, line 9, with the following rewritten paragraph:

1 After the CPS-packet(s) have been encapsulated on an CPS-packet
2 boundary, the AAL2 Rx DMA 515 will write the data into either Rx FIFO A 540,
3 Rx FIFO B 541, or the Rx Host FIFO 530. By monitoring the FIFO's read and
4 write pointers, the DSP 412 ~~460~~ and host 414 ~~490~~ can determine when CPS
5 packets are available to them.

Please replace the paragraph beginning at page 40, line 1, with the following rewritten paragraph:

1 Further, communication between the functional blocks (i.e. DSP 412 ~~460~~,
2 host 414 ~~490~~ and AAL2 950) are minimized due to the fact that the protocol
3 between the functions is drastically simplified with the AAL2 Receiver 950
4 directly interfaced with the DSP 412 ~~460~~. Latency is minimized because of the
5 direct connection to the DSP FIFO. The data is only written once across the
6 system bus. An end result is overall improved system performance.

Please replace the paragraph beginning at page 42, line 15, with the following rewritten paragraph:

1 Status signals 612 and 614 interface directly to the PDSP's status
2 register. When the signals are asserted (set to high), the ATM Processor 120 is
3 notified that cells are available to either be buffered (i.e. Cell Buffer OUT Queue
4 616 is empty) or cells can be fetched and forwarded to the Cell DMA I/F (i.e. at
5 least one of the ports' IN queues 617 are not empty). When the IN queue status
6 bit is set, the PDSP 114 reads the IN Queue Status register in order to determine
7 which IN queues 617 contain an ATM cell.

Please replace the paragraph beginning at page 43, line 3, with the following rewritten paragraph:

1 The memory of the Cache 615 is preferably a Dual-Port RAM, used as a
2 cache between the PDSP 114 and SDRAM (located off chip) or other similar
3 remote memory device, the SDRAM is accessible through the chip/peripheral
4 interface. The cache 615 can be logically partitioned into a plurality of queues
5 616, 617, ~~queue~~ each queue containing N cells (RAM sized based on the
6 application).

Please replace the paragraph beginning at page 43, line 8, with the following rewritten paragraph:

1 When an ATM cell needs to be buffered, the PDSP 114 writes the cell into
2 the Cell Buffer Cache's OUT queue 616. The ATM cell contains certain port and
3 queue information which is contained in the last three bytes of a 32-bit bounded
4 ATM cell. This information is used by the cache DMA 620 to forward the cell to
5 the correct queue. Figure 7 illustrates an exemplary aligned ATM cell in
6 accordance with the present invention.

Please replace the paragraph beginning at page 44, line 9, with the following rewritten paragraph:

1 Before a cell is written into the OUT queue 616 of the cache 615, the
2 PDSP 114 appends a Cache Queue ID into the last three bytes of a 32-bit
3 bounded ATM cell. Since the transfers across the Memory Bus are is performed
4 in 32-bit words, the ATM cell resides in byte 1 through 53 while bytes 54, 55, and
5 56 are unused.

Please replace the paragraph beginning at page 44, line 16, with the following rewritten paragraph:

1 The cache DMA 620 services the OUT queue 616 (i.e. cells to be
2 buffered) and the IN queues 617 (i.e. cells to be fetched) for all queues. This is
3 accomplished by the cache DMA 620 moving ATM cells from the cache 615 out
4 to the SDRAM (if the IN queues are full) as well as moving ATM cells from the
5 SDRAM into the cache 615.

Please replace the paragraph beginning at page 45, line 3, with the following rewritten paragraph:

1 The cache DMA 620 uses internal queue pointers to determine if a cell
2 can be moved from the OUT queue and into either an IN queue in the memory
3 614 or the external memory (e.g. SDRAM). The highest priority of the cache
4 DMA 620 is to service the OUT queue 616 ~~containing~~ contains a cell, the Port
5 and Queue ID is interrogated then the cache logic determines if the cell is
6 forwarded to the IN queue 617 or SDRAM, or left in the OUT queue 616. The
7 particular IN queue's cache occupancy is checked, and if cache queue is not full
8 then the cell is immediately written into the IN queue 617 in the cache 615. If the
9 cache queue is full, then the cell is forwarded to the external queue in the
10 SDRAM. Note that the cell is only forwarded to the external queue in the
11 SDRAM if the IN queue 617 in the cache 615 is full.

Please replace the paragraph beginning at page 45, line 13, with the following rewritten paragraph:

1 The cache DMA 620 is the master of the cells buffered in the external
2 queues. If there is not a cell in the OUT queue 616 and an IN queue 617 in the
3 cache 615 is not full, the DMA 620 moves a cell from the external queues into
4 the cache 615. Thus, the IN queues 617 ~~queue~~ associated with the cache 615
5 are fully occupied before the external queues are utilized.

Please replace the paragraph beginning at page 46, line 4, with the following rewritten paragraph:

1 The Cell Buffer Module 600 can be implemented in hardware and,
2 therefore, is easily implemented and can virtually be “dropped” into any “system-
3 on-a-chip”. Further, the Cache 600 is scalable. That is, the module easily scales
4 to a specific system requirement as far as number of ports & levels of priority
5 supported, as well as PDU depth on the IN/OUT Queues 616, 617. Also, priority
6 assigned per queue is easily adapted since a priority algorithm is executed from
7 the ATM processor 120 or switching engine.

IN THE ABSTRACT:

Please replace Page 56 with the accompanying substitute Page 56, in which the paragraph beginning at page 56, line 2, has been replaced with the following rewritten paragraph:

1 The present invention provides an apparatus and system for high speed
2 end-to-end telecommunication traffic using an Asynchronous Transfer Mode
3 (ATM) architecture for convergence of video, data and voice in an SOHO
4 application using a DSL router. An ATM processor (120) enables traffic shaping,
5 and operation and maintenance processing within a single module. The ATM
6 processor (120) further includes a processor (114) which executes firmware from
7 a program memory (110). A register block (116) is provided for communicating
8 setup and teardown notification, and OAM configuration to the processor (114)
9 and a connection state RAM (112) ~~(12)~~ provides for communicating connection
10 configuration in which this information is used by the processor (114) when
11 performing the functions of switching, QoS, and OAM. Transmit scheduler
12 hardware (118) is provided for the scheduling of ATM cell transmission and is
13 configured by the processor (114).